CLAIMS

1. Metal interconnect lines for integrated circuits, the lines comprising:

a first copper layer; and

a second aluminum layer.

2. The metal interconnect lines of claim 1 wherein the copper layer has been electroplated into a channel etched in an dielectric layer of the integrated circuit.

3. The metal interconnect lines of claim 2 wherein a mask is used to pattern the dielectric before etching the channel in the oxide layer.

4. The metal interconnect line of claim 3 wherein the same mask is used to pattern the aluminum after deposition on the copper layer as was used to pattern the dielectric layer.

5. The metal interconnect line of claim 1 wherein a thin barrier layer is placed between the first copper layer and the second aluminum layer.

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6. A method for fabricating low resistance interconnect lines in an integrated circuit, the method comprising the steps of:

patterning and etching a dielectric layer in an integrated circuit;

filling the etched areas of the dielectric layer with a first conductive material;

depositing a second conductive material on the first conductive material;

patterning and etching the second conductive material so that the second conductive material overlies only areas filled with the first conductive material.

7. The method of claim 6 wherein the same mask used to pattern the dielectric layer is used to pattern the second conductive material.

8. The method of claim 6 wherein the first conductive material is copper and the second conductive material is aluminum.

9. The method of claim 8 wherein a barrier material is deposited atop the copper before the aluminum is deposited and patterned.

10. The method of claim 8 wherein the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance.

add a^2

add c1